WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device, comprising:

a memory cell unit including at least one memory cell transistor formed on a semiconductor substrate and having a laminated structure of a charge accumulation layer and a control gate layer; and

a selection gate transistor one of the source/drain diffusion layer regions of which is connected to a bit line or a source line and the other of the the source/drain diffusion layer regions of which is connected to the memory cell unit,

wherein the shape of the source diffusion layer region of the selection gate transistor is asymmetical to the shape of the drain diffusion layer region thereof below the selection gate transistor.

2. A non-volatile semiconductor memory device according to claim 1, wherein the distance, where the diffusion layer region connected to the bit line or the source line overlaps the gate electrode, is made smaller than the distance, where the diffusion layer region connected to the memory cell transistor overlaps the gate electrode, at the positions thereof which have the same depth from the boundary between the semiconductor substrate and a gate insulation film.

3. A non-volatile semiconductor memory device according to claim 1, wherein the deepest portion of

the diffusion layer region connected to the bit line or the source line is made shallower than the deepest portion of the diffusion layer region connected to the memory cell unit below the gate electrode.

4. A non-volatile semiconductor memory device according to claim 1, wherein the effective concentration of impurity of the diffusion layer region connected to the bit line or the source line is made lower than the effective concentration of impurity of the diffusion layer region connected to the memory cell unit at the positions thereof which have the same depth from the boundary between the semiconductor substrate and the gate insulation film.

5. A non-volatile semiconductor memory device according to claim 1, wherein the effective concentration of impurity of the diffusion layer region connected to the memory cell unit is the same as the the effective concentration of impurity of the source/drain diffusion layer region of the memory cell transistor at the positions thereof which have the same depth from the boundary between the semiconductor substrate and the gate insulation film.

6. A non-volatile semiconductor memory device according to claim 1, wherein a contact for connecting the bit line or the source line to the diffusion layer region is formed in self-alignment with respect to the gate electrode of the selection gate transistor.

7. A non-volatile semiconductor memory device according to claim 1, wherein the memory device comprises:

a first insulation film, a second insulation film formed on the first insulation film, and a third insulation film formed on the second insulation film are laminated on the sidewalls of the gate electrode of the memory cell transistor and on the gate electrode of the selection gate transistor on the side thereof facing the memory cell; and

the first insulation film, and the third insulation film formed on the first insulation film are laminated on the gate electrode of the selection gate transistor on the side thereof facing the contact for connecting the bit line or the source line.

8. A non-volatile semiconductor memory device, comprising:

a memory cell unit including at least one memory cell transistor formed on a semiconductor substrate and having a laminated structure of a charge accumulation layer and a control gate layer; and

a selection gate transistor one of the source/drain diffusion layer regions of which is connected to a bit line or a source line and the other of the the source/drain diffusion layer regions of which is connected to the memory cell unit,

wherein the channel region between the source

diffusion layer region of the selection gate transistor and the drain diffusion layer region thereof includes a region having a different concentration of impurity at the positions thereof which have the same depth from the boundary between the semiconductor substrate and a gate insulation film.

9. A non-volatile semiconductor memory device according to claim 8, wherein, in the channel region of the selection gate transistor, the concentration of impurity of the channel region in contact with the diffusion layer region connected to the bit line or the source line is higher than the concenration of impurity of the channel region in contact with the diffusion layer region connected to the memory cell unit at the positions thereof which have the same depth from the boundary between the semiconductor substrate and the gate insulation film.

10. A non-volatile semiconductor memory device according to claim 8, wherein the concenration of impurity of the channel region in contact with the diffusion layer region connected to the memory cell unit is the same as the concenration of impurity of the channel region in contact with the source/drain diffusion layer region of the memory cell unit at the positions thereof which have the same depth from the boundary between the semiconductor substrate and the gate insulation film.

11. A non-volatile semiconductor memory device according to claim 8, wherein a contact for connecting the bit line or the source line to the diffusion layer region is formed in self-alignment with respect to the gate electrode of the selection gate transistor.

12. A non-volatile semiconductor memory device according to claim 8, wherein the memory device comprising:

a first insulation film, a second insulation film formed on the first insulation film, and a third insulation film formed on the second insulation film are laminated on the sidewalls of the gate electrode of the memory cell transistor and on the gate electrode of the selection gate transistor on the side thereof facing the memory cell; and

the first insulation film, and the third insulation film formed on the first insulation film are laminated on the gate electrode of the selection gate transistor on the side thereof facing the contact for connecting the bit line or the source line.

13. A method of manufacturing a non-volatile semiconductor memory device, comprising:

a step of forming gate electrodes of a memory cell transistor and a selection gate transistor having a first conductive type channel region on a semiconductor substrate;

a step of forming a mask having an aperture on

the side of the gate electrode of the selection gate transistor opposite to the side thereof facing the memory cell transistor; and

a step of implanting a first conductive type impurity in the semiconductor substrate through the aperture of the mask.

14. A method of manufacturing a non-volatile semiconductor memory device, comprising:

a step of forming gate electrodes of a memory cell transistor and a selection gate transistor having a first conductive type channel region on a semiconductor substrate;

a step of forming a first insulation film on the sidewalls of the gate electrodes of the memory cell transistor and the selection gate transistor;

a step of forming a second insulation film on the first insulation film;

a step of forming a mask having an aperture on the side of the gate electrode of the selection gate transistor opposite to the side thereof facing the memory cell transistor;

a step of removing the second insulation film through the aperture of the mask; and

a step of implanting a first conductive type impurity in the semiconductor substrate through the aperture of the mask.

15. A method of manufacturing a non-volatile

semiconductor memory device, comprising:

a step of forming gate electrodes of a memory cell transistor and a selection gate transistor having a first conductive type channel region on a semiconductor substrate;

a step of opening a contact hole through the source/drain diffusion layer region of the selection gate transistor in self-alignment with respect to the gate electrode of the selection gate transistor; and

a step of implanting a first conductive type impurity in the semiconductor substrate through the contact hole.

16. A method of manufacturing a non-volatile semiconductor memory device according to claim 13, wherein the impurity is implanted at an angle so that the impurity is implanted in the channel region below the gate electrode of the selection gate transistor.

17. A method of manufacturing a non-volatile semiconductor memory device, comprising:

a step of forming gate electrodes of a memory cell transistor and selection gate transistors having a first conductive type channel region on a semiconductor substrate in such a manner that the space between the gate electrodes of the selection gate transistors is set larger than the space between the gate electrode of the memory cell transistor and the gate electrode of a selection gate transistor; and

a step of implanting a first conductive type impurity in the semiconductor substrate at such an angle that the impurity is not implanted between the gate electrode of the memory cell transistor and the gate electrode of the selection gate transistor and is implanted between the gate electrodes of the selection gate transistors.

18. A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell having a laminated gate structure of a charge accumulation layer and a control gate layer formed on a semiconductor substrate through a gate insulation film; and

a plurality of selection gate transistors each having a gate electrode formed through the gate insulation film and a source/drain diffusion layer one of which is connected to each memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate transistors include a pair of first selection gate transistors disposed in confrontation with each other across a contact portion connected to the bit line or to the source line and having substantially the same structure; and

the channel regions of the pair of selection gate

transistors have the same impurity concentration in a gate length direction at a depth equal from the boundary between the semiconductor substrate and the gate insulation film as well as the concentration distribution of impurity in the channel regions of the pair of selection gate transistors is different from that of the channel region of the memory cell.

19. A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell having a laminated gate structure of a charge accumulation layer and a control gate layer formed on a semiconductor substrate through a gate insulation film; and

a plurality of selection gate transistors each having a gate electrode formed through a gate insulation film formed of the same layer as the gate insulation film of the memory cell and a source/drain diffusion layer one of which is connected to each memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate transistors have a pair of first selection gate transistors disposed in confrontation with each other across a contact portion connected to the bit line or to the source line and having substantially the same structure; and

the effective impurity concentration of the source/drain diffusion layer of the pair of first selection gate transistors is lower than that of the source/drain diffusion layer of the memory cell at a depth equal from the boundary between the semiconductor substrate and the gate insulation film.

20. A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell having a laminated gate structure of a charge accumulation layer and a control gate layer formed on a semiconductor substrate through a gate insulation film; and

a plurality of selection gate transistors each having a gate electrode formed through a gate insulation film formed of the same layer as the gate insulation film of the memory cell and a source/drain diffusion layer one of which is connected to each memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate transistors have first selection gate transistors and second selection gate transistors disposed in confrontation with each other through a contact portion connected to the bit line or the source line, and the structure of the first selection gate transistors is substantially different from that of the second

selection gate transistors;

the channel regions of the first selection gate transistors have the same impurity concentration in a gate length direction at a depth equal from the boundary between the semiconductor substrate and the gate insulation film as well as the concentration distribution of impurity of the channel regions of the first selection gate transistors is different from that of the channel region of the memory cell; and

each of the second selection gate transistors has a portion in which the impurity concentration of the channel region thereof is different in a gate length direction at the above depth from the boundary between the semiconductor substrate, and the impurity concentration of the portion of the channel region containing a high concentration impurity is the same as that of the channel region of each of the first selection gate transistors at the above depth from the boundary between the semiconductor substrate and the gate insulation film.

21. A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell having a laminated gate structure of a charge accumulation layer and a control gate layer formed on a semiconductor substrate through a gate insulation film; and

a plurality of selection gate transistor each having a gate electrode formed through a gate insulation film that is formed simultaneously with the gate insulation film of the memory cell and a source/drain diffusion layer one of which is connected to each memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate transistors have first selection gate transistors and second selection gate transistors disposed in confrontation with each other through a contact portion connected to the bit line or the source line, and the structure of the first selection gate transistors is substantially different from that of the second selection gate transistors;

the impurity concentration of the source diffusion layer of each of the first selection gate transistors is the same as that of the drain diffusion layer thereof at a depth equal from the boundary between the semiconductor substrate and the gate insulation film as well as the effective impurity concentration of the source/drain diffusion layer of each of the first selection gate transistors is lower than that of the source/drain diffusion layer of the memory cell; and

the impurity concentration of the source diffusion layer of each of the second selection gate transistors is different from that of the drain diffusion layer

thereof at a depth equal from the boundary between the semiconductor substrate and the gate insulation film as well as the impurity concentration of the source diffusion layer or the drain diffusion layer, which is connected to the bit line or the source line, of each of the second selection gate transistors is the same as that of the source/drain diffusion layer of each of the first selection gate transistors.

22. A non-volatile semiconductor memory device according to claim 18, wherein the impurity concentration of the channel region of each of the first selection gate transistors is made higher than that of the channel region of the memory cell.

23. A non-volatile semiconductor memory device according to claim 18, wherein the impurity distribution width of the channel region of each of the first selection gate transistors is narrower than that of the channel region of the memory cell at a depth equal from the boundary between the semiconductor substrate and the gate insulation film.

24. A non-volatile semiconductor memory device according to claim 19, wherein the distance, where the source/drain diffusion layer of each selection gate transistor overlaps the gate electrode thereof, is made smaller than the distance, where the source/drain diffusion layer of the memory cell overlaps the gate electrode thereof at the depth from the boundary

between the semiconductor substrate and the gate insulation film.

25. A non-volatile semiconductor memory device according to claim 19, wherein the junction depth of the source/drain diffusion layer of each of the first selection gate transistors from the boundary between the semiconductor substrate and the gate insulation film is made smaller than the junction depth of the source/drain diffusion layer of the memory cell from the boundary between the semiconductor substrate and the gate insulation film.

26. A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell having a laminated gate structure of a charge accumulation layer and a control gate layer formed on a semiconductor substrate through a gate insulation film; and

a plurality of selection gate transistor each having a gate electrode formed through a gate insulation film that is formed simultaneously with the gate insulation film of the memory cell and is substantially the same therewith and a source/drain diffusion layer one of which is connected to each memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate

transistors have a pair of selection gate transistors disposed in confrontation with each other across a contact portion connected to the bit line or to the source line; and

the pair of selection gate transistors have substantially the same structure, each of the pair of transistors has a portion in which the impurity concentration of the channel region thereof is different in a gate length direction at a depth equal from the boundary between the semiconductor substrate and the gate insulation film, and the concentration distribution of impurity of the channel region of each transistor is different from that of the channel region of the memory cell.

27. A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell formed on a semiconductor substrate through a gate insulation film and having a laminated gate structure of a charge accumulation layer and a control gate layer; and

a plurality of selection gate transistor each having a gate electrode formed through a gate insulation film that is formed simultaneously with the gate insulation film of the memory cell and is substantially the same therewith and a source/drain diffusion layer one of which is connected to each

memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate transistors have a pair of selection gate transistors disposed in confrontation with each other across a contact portion connected to the bit line or to the source line and having substantially the same structure; and

the impurity concentration of the source diffusion layer of each of the pair of selection gate transistors is different from that of the drain diffusion layer thereof at a depth equal from the boundary between the semiconductor substrate and the gate insulation film as well as the effective impurity concentration of the source diffusion layer or the drain diffusion layer, which is connected to the bit line or the source line, of each selection gate transistor is lower than that the source/drain diffusion layer of the memory cell.

28. A non-volatile semiconductor memory device according to claim 26, wherein the impurity concentration of the portion of the channel region of each selection gate transistor on one of the bit line contact portion side thereof and the source line contact portion side thereof is made higher than the impurity concentration of the channel region of the memory cell at the above depth from the boundary between the semiconductor substrate and the gate

insulation film.

29. A non-volatile semiconductor memory device according to claim 26, wherein the impurity distribution width of the portion of the channel region of each selection gate transistor on one of the bit line contact portion side therof and the source line contact portion side thereof is made smaller than the impurity distribution width of the channel region of the memory cell at the above depth from the boundary between the semiconductor substrate and the gate insulation film.

30. A non-volatile semiconductor memory device according to claim 27, wherein the distance, where the source/drain diffusion layer, which is connected to the bit line or to the source line, of each selection gate transistor overlaps the gate electrode thereof, is made smaller than the distance,where the source/drain diffusion layer of the memory cell overlaps the gate electrode thereof at the above depth from the boundary between the semiconductor substrate and the gate insulation film.

31. A non-volatile semiconductor memory device according to claim 27, wherein the junction depth of the source/drain diffusion layer, which is connected to the bit line or to the source line, of each selection gate transistor from the boundary between the semiconductor substrate and the gate insulation film is

made smaller than that of the source/drain diffusion layer of the memory cell from the boundary between the semiconductor substrate and the gate insulation film.

32. A non-volatile semiconductor memory device according to claim 18, wherein the impurity concentration of each selection gate transistor in the vicinity of the depth of element isolation regions in the depth direction of the activation region of the selection gate transistor is the same as the impurity concentration in the semiconductor substrate just below an element isolation region surrounding at least one transistor constituting a peripheral circuit.

33. A non-volatile semiconductor memory device according to claim 18, wherein the distance between the gate electrode of each selection gate transistor and the gate electrode of the memory cells is made larger than the distance between the gate electrodes of the memory cells.

34. A non-volatile semiconductor memory device according to claim 18, wherein a part of the source/drain diffusion layer of each selection gate transistor and a part of the source/drain diffusion layer have such a structure that they are connected to each other through a continuous activation region without being isolated from each other by an element isolation region.

35. A method of manufacturing a non-volatile

semiconductor memory device, comprising:

forming the first conductive type channel regions of a memory cell and selection gate transistors on the surface of a semiconductor substrate;

forming an impurity doping mask having apertures corresponding to only the channel regions of the selection gate transistors on the semiconductor substrate; and

doping a first conductive type impurity in the semiconductor substrate through the mask.

36. A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming first conductive type channel regions of a memory cell and selection gate transistors on the surface of a semiconductor substrate;

forming a gate insulation film on the semiconductor substrate;

forming a part of gate electrodes on the gate insulation film;

forming element isolation regions on the surface layer portion of the semiconductor substrate in self-alignment using the part of gate electrodes as a mask;

forming an impurity doping mask having apertures corresponding to only the channel regions the selection gate transistors on the semiconductor substrate; and

doping a first conductive type impurity in the semiconductor substrate via the part of the gate

semiconductor memory device, comprising:

forming the first conductive type channel regions of a memory cell and selection gate transistors on the surface of a semiconductor substrate;

forming an impurity doping mask having apertures corresponding to only the channel regions of the selection gate transistors on the semiconductor substrate; and

doping a first conductive type impurity in the semiconductor substrate through the mask.

36. A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming first conductive type channel regions of a memory cell and selection gate transistors on the surface of a semiconductor substrate;

forming a gate insulation film on the semiconductor substrate;

forming a part of gate electrodes on the gate insulation film;

forming element isolation regions on the surface layer portion of the semiconductor substrate in self-alignment using the part of gate electrodes as a mask;

forming an impurity doping mask having apertures corresponding to only the channel regions the selection gate transistors on the semiconductor substrate; and

doping a first conductive type impurity in the semiconductor substrate via the part of the gate

electrodes through the mask.

37. A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming first conductive type channel regions of a memory cell and selection gate transistors on the surface of a semiconductor substrate;

forming a gate insulation film on the semiconductor substrate;

forming a part of gate electrodes on the gate insulation film;

forming element isolation regions on the surface layer portion of the semiconductor substrate in self-alignment using the part of the gate electrodes as a mask;

forming an impurity doping mask having apertures corresponding to the channel regions the selection gate transistors and to the element isolation region of a transistor constituting the peripheral circuit of memory cell units; and

doping a first conductive type impurity in the semiconductor substrate via the part of the gate electrodes through the mask.